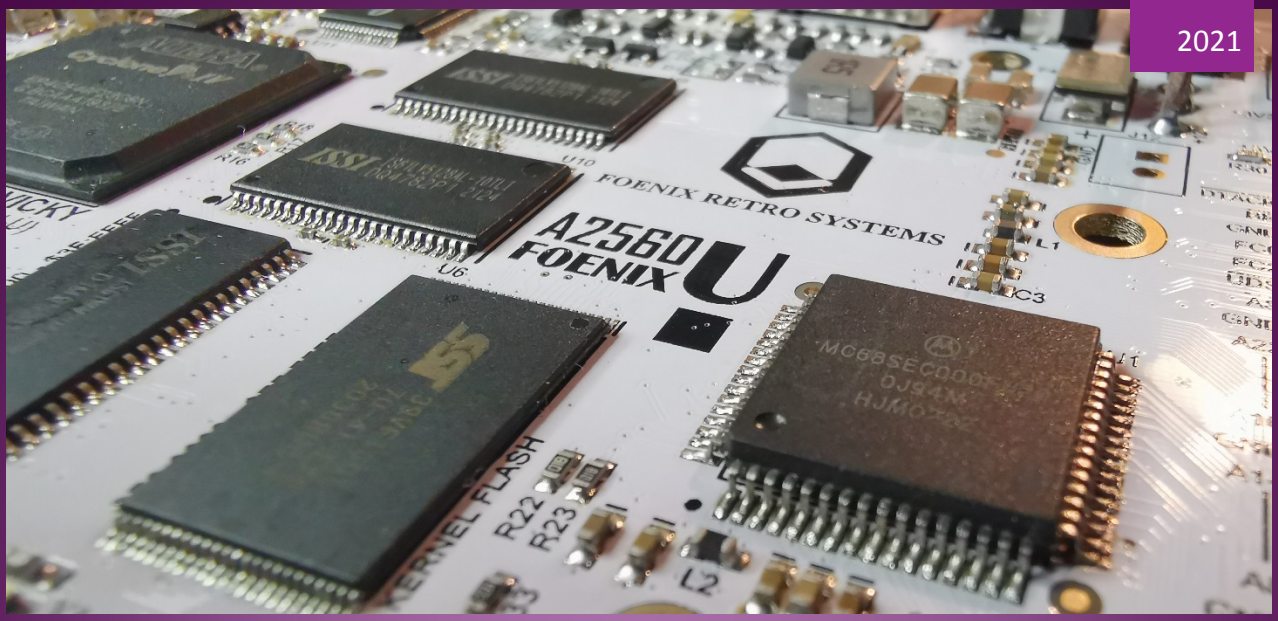
2021



A2560 Foenix U

USER MANUAL

REVISION 0.0.2

FOENIX RETRO SYSTEMS

Revision History		By	Rev	Date
Alpha Release - Preliminary		Stefany Allaire	0.0.0	Nov 16th, 2021
RTC Registers / Interrupt Vector Update		Stefany Allaire	0.0.1	Dec 11th, 2021
Timer Registers Update		Stefany Allaire	0.0.2	Dec 21st, 2021

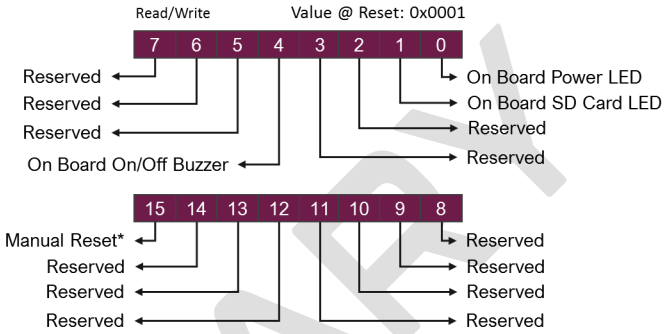
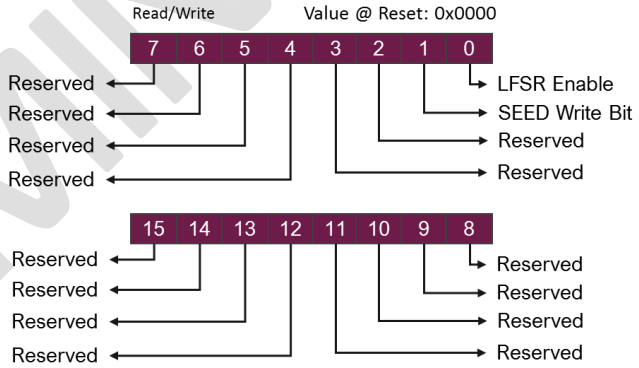
Block Diagram

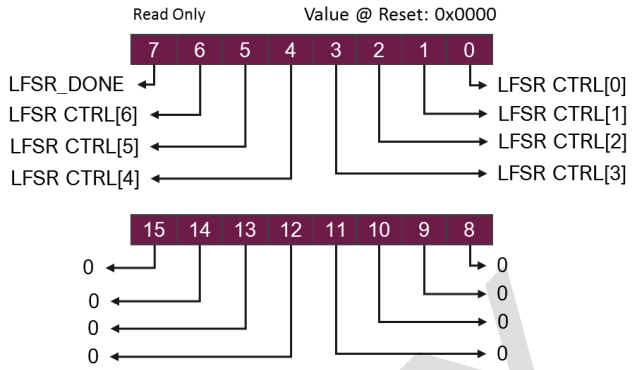
Memory Map

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x000000	0x3FFFFF	8/16	MEM	R/W	System RAM - SRAM – 4Meg
0x400000	0xAFFFFF	-	-	-	Empty Space (will trigger an BERR if accessed)
0xB00000	0xB1FFFF	8/16/32	I/O	R/W	GAVIN Registers (System Controller)
0xB20000	0xB3FFFF	8/16/32	I/O	R/W	BEATRIX Registers (Sound/Music/DAC)
0xB40000	0xB5FFFF	8/16/32	I/O	R/W	VICKY II Registers (Text/Graphics Controller)
0xB60000	0xB63FFF	8/16	MEM	R/W	Text Memory Block
0xB64000	0xB67FFF	8/16	MEM	R/W	Text Color Memory Block
0xBF0000	0xBFFFFF	8/16	I/O/MEM	R/W	Expansion Bus Chip Select
0xC00000	0xDFFFFF	32	MEM	R/W	Video RAM – SRAM – 2Meg
0xE00000	0xFFFFFF	16	MEM	R	FLASH – 2Meg

GAVIN Address Offset: 0x00B0

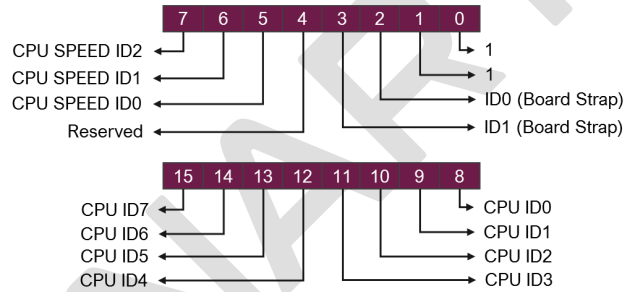
1. System Control Register

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x0000		16	I/O	R/W	**GAVIN Control Register** 
0x0002		16	I/O	R/W	**Manual Reset - * Security Word** Value @ Reset: 0x0000 Write the Value: 0xDEAD to unlock the Manual Reset
0x0004		16	I/O	R/W	**LFSR Control Register** 
0x0006		16	I/O	R/W	**LFSR SEED Value** Write a Value to setup the LFSR Seed, then set bit#1 of LFSR Control Register. Then, clear the bit. This will latch the value of the Seed in the LFSR.
0x0008		16	I/O	R	**LFSR Output Value** Every time you read this register after the LFSR has been enabled and the Seed setup, you will get a new random value.
0x000A		16	I/O	R	**LFSR Status Register**



0x000C | | **16** | **I/O** | **R**

Machine ID



Possible Value for Machine ID:

Machine	Bit 3	Bit 2	Bit 1	Bit 0
FMX	**0**	**0**	**0**	**0**
C256U	**0**	**0**	**0**	**1**
Reserved	**0**	**0**	**1**	**0**
A2560 Dev	**0**	**0**	**1**	**1**
GEN X	**0**	**1**	**0**	**0**
C256U+	**0**	**1**	**0**	**1**
Reserved	**0**	**1**	**1**	**0**
Reserved	**0**	**1**	**1**	**1**
A2560X	**1**	**0**	**0**	**0**
A2560U	**1**	**0**	**0**	**1**
Reserved	**1**	**0**	**1**	**0**
A2560K	**1**	**0**	**1**	**1**

Possible Value for CPU Speed ID:

	SPEED ID		
CPU SPEED ID	2	1	0
14.318Mhz	0	0	0
20.000Mhz	0	0	1
25.000Mhz	0	1	0
33.000Mhz	0	1	1
40.000Mhz	1	0	0
50.000Mhz	1	0	1
66.000Mhz	1	1	0
80.000Mhz	1	1	1

Possible Value for CPUID:

	CPU Model				Speed Grade			
CPU	7	6	5	4	3	2	1	0
MC68SEC000	0	0	0	0	X	X	X	X
MC68020	0	0	0	1	X	X	X	X
MC68EC020	0	0	1	0	X	X	X	X
MC68030	0	0	1	1	X	X	X	X
MC68EC30	0	1	0	0	X	X	X	X
MC68040	0	1	0	1	X	X	X	X
MC68040V	0	1	1	0	X	X	X	X
MC68EC40	0	1	1	1	X	X	X	X
486DX2-50	1	0	0	0	0	0	0	0
486DX2-66	1	0	0	0	0	0	0	1
486DX4	1	0	0	1	X	X	X	X

0x000E		**16**	**I/O**	**R/W**	**Reserved – Future Expansion**
0x0010		**16**	**I/O**	**R**	**Byte Order Hi** Value @ Reset: **0x4567**
0x0012		**16**	**I/O**	**R**	**Byte Order Lo** Value @ Reset: **0x0123**
0x0014		**16**	**I/O**	**R**	**Reserved** Value @ Reset: 0x0000
0x0016		**16**	**I/O**	**R**	**Reserved** Value @ Reset: 0x0000
0x0018		**16**	**I/O**	**R**	**Reserved** Value @ Reset: 0x0000
0x001A		**16**	**I/O**	**R**	**Reserved** Value @ Reset: 0x0000
0x001C		**16**	**I/O**	**R**	**Reserved** Value @ Reset: 0x0000
0x001E		**16**	**I/O**	**R**	**Reserved** Value @ Reset: 0x0000

2. Real Time Clock

(For Detailed information, please consult the BQ4802LY Datasheet)

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x0080		8	I/O	R/W	**RTC – Seconds Register**
0x0082		8	I/O	R/W	**RTC – Seconds Alarm**
0x0084		8	I/O	R/W	**RTC – Minutes Register**
0x0086		8	I/O	R/W	**RTC – Minutes Alarm**
0x0088		8	I/O	R/W	**RTC – Hours Register**
0x008A		8	I/O	R/W	**RTC – Hours Alarm**
0x008C		8	I/O	R/W	**RTC – Day**
0x008E		8	I/O	R/W	**RTC – Day Alarm**
0x0090		8	I/O	R/W	**RTC – Day of Week**
0x0092		8	I/O	R/W	**RTC – Month**
0x0094		8	I/O	R/W	**RTC – Year**
0x0096		8	I/O	R/W	**RTC – Rates**

RTC – Seconds Register

	10 Sec Digit				1 Sec Digit			
	7	6	5	4	3	2	1	0
Seconds (00-59)	0	T	T	T	U	U	U	U

- T = Tens, U = Units

RTC – Seconds Alarm

		10 Sec Digit			1 Sec Digit			
	7	6	5	4	3	2	1	0
Seconds alarm	ALM1	ALM0	T	T	U	U	U	U
Seconds alarm		T	T	T	U	U	U	U

- T = Tens, U = Units

RTC – Minutes Register

	10 Min Digit				1 Min Digit			
	7	6	5	4	3	2	1	0
Minutes (00-59)	0	T	T	T	U	U	U	U

- T = Tens, U = Units

RTC – Minutes Alarm

		10 Min Digit			1 Sec Digit			
	7	6	5	4	3	2	1	0
Minutes alarm	ALM1	ALM0	T	T	U	U	U	U
Minutes alarm		T	T	T	U	U	U	U

- T = Tens, U = Units

RTC – Hours Register

		10 Hour Digit			1 Hour Digit			
	7	6	5	4	3	2	1	0
Hours (01-12AM) Hours (81-92PM)	PM/AM	0	T	T	U	U	U	U

- T = Tens, U = Units

RTC – Hours Alarm

		10 Hour Digit			1 Hour Digit			
	7	6	5	4	3	2	1	0
Hours (01-12AM) Hours (81-92PM)	PM/AM ALM1	ALM0	T	T	U	U	U	U

- T = Tens, U = Units

RTC – Day

		10 Day Digit			1 Day Digit			
	7	6	5	4	3	2	1	0
Day (01-31)	0	0	T	T	U	U	U	U

- T = Tens, U = Units

RTC – Day Alarm

		10 Day Digit			1 Day Digit			
	7	6	5	4	3	2	1	0
Day (01-31)	ALM1	ALM0	T	T	U	U	U	U

- T = Tens, U = Units

RTC – Day of Week

						Day of Week		
	7	6	5	4	3	2	1	0
Day of Week (01-07)	0	0	0	0	0	U	U	U

- U = Units

RTC – Month

					Month Digit			
	7	6	5	4	3	2	1	0
Month (01-12)	0	0	0	T	U	U	U	U

- T = Tens, U = Units

RTC – Year

	10 Year Digit				1 Year Digit			
	7	6	5	4	3	2	1	0
Years (99-00)	T	T	T	T	U	U	U	U

- T = Tens, U = Units

RTC – Rates

	7	6	5	4	3	2	1	0
Rates	0	WD2	WD1	WD0	RES3	RES2	RES1	RES0

0x0098		**8**	**I/O**	**R/W**	**RTC – Enables**

	7	6	5	4	3	2	1	0
Enables	0	0	0	0	AIE	PIE	PWRIE	ABE

0x009A		**8**	**I/O**	**R/W**	**RTC – Flags**

	7	6	5	4	3	2	1	0
Flags	0	0	0	0	AF	PF	PWRF	BVF

0x009C		**8**	**I/O**	**R/W**	**RTC – Control**

	7	6	5	4	3	2	1	0
Control	0	0	0	0	UTI	STOPn	24/12	DSE

0x009E		**8**	**I/O**	**R/W**	**RTC – Century**

	10 Year Digit				1 Year Digit			
	7	6	5	4	3	2	1	0
Century (99-00)	T	T	T	T	U	U	U	U

T = Tens, U = Units

3. Interrupt Controller Registers

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x0100		16	I/O	R/W	**Interrupt Pending Register Group 0 (VICKY)**

Interrupt Source	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VICKY INT0 (SOF)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
VICKY INT1 (SOL)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
VICKY INT2 (Sprite Collision)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
VICKY INT3 (Bitmap Collision)	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
VICKY INT4 (VDMA Interrupt)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
VICKY INT5 (Tile Collision)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
VICKY Hot-Plug	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Value @ Reset: 0x0000

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x0102		16	I/O	R/W	**Interrupt Pending Register Group 1 (GAVIN)**

Interrupt Source	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PS2 Keyboard	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PS2 Mouse	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
COM1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Timer 0 (CPU Clock)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Timer 1 (CPU Clock)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Timer 2 (CPU Clock)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Timer 3 (SOF Clock)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RTC	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Value @ Reset: 0x0000

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x0104		16	I/O	R/W	**Interrupt Pending Register Group 2 (BEATRIX)**

Interrupt Source	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
SDCard Insert	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OPL3	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BTX INT0 (TBD)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BTX INT1 (TBD)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BTX INT2 (TBD)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BTX INT3 (TBD)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DAC0 Playback	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Value @ Reset: 0x0000

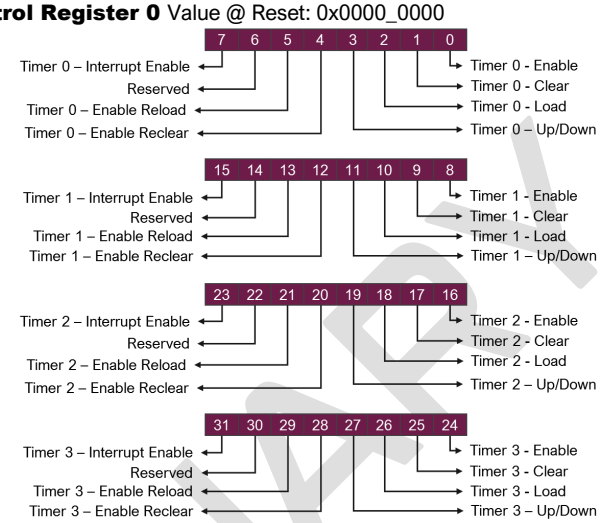
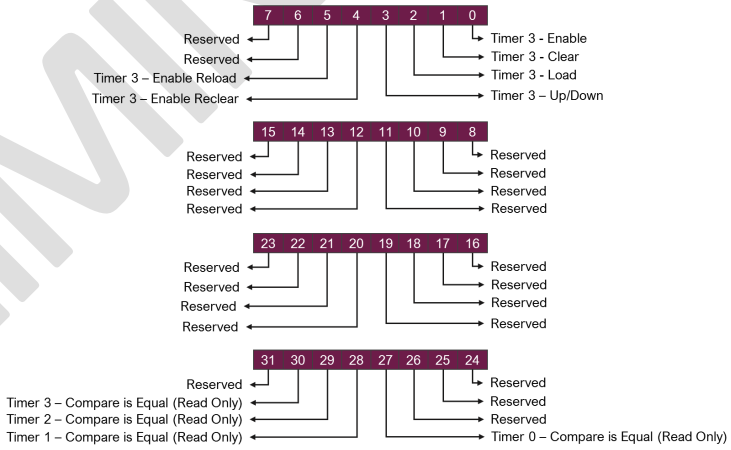
Addy Start Offset	Addy End	Size	Type	R/W	Description
0x0106		16	I/O	R/W	**Reserved**

0x0108		**16**	**I/O**	**R/W**	**Polarity Register Group 0 (Not in Use)** Value @ Reset: 0x0000
0x010A		**16**	**I/O**	**R/W**	**Polarity Register Group 1 (Not in Use)** Value @ Reset: 0x0000
0x010C		**16**	**I/O**	**R/W**	**Polarity Register Group 2 (Not in Use)** Value @ Reset: 0x0000
0x010E		**16**	**I/O**	**R/W**	**Reserved**
0x0110		**16**	**I/O**	**R/W**	**EDGE Register Group 0 (Not in Use)** Value @ Reset: 0xFFFF
0x0112		**16**	**I/O**	**R/W**	**EDGE Register Group 1 (Not in Use)** Value @ Reset: 0xFFFF
0x0114		**16**	**I/O**	**R/W**	**EDGE Register Group 2 (Not in Use)** Value @ Reset: 0xFFFF
0x0116		**16**	**I/O**	**R/W**	**Reserved**
0x0118		**16**	**I/O**	**R/W**	**MASK Register Group 0** Value @ Reset: 0xFFFF
0x011A		**16**	**I/O**	**R/W**	**MASK Register Group 1** Value @ Reset: 0xFFFF
0x011C		**16**	**I/O**	**R/W**	**MASK Register Group 2** Value @ Reset: 0xFFFF
0x011E		**16**	**I/O**	**R/W**	**Reserved**

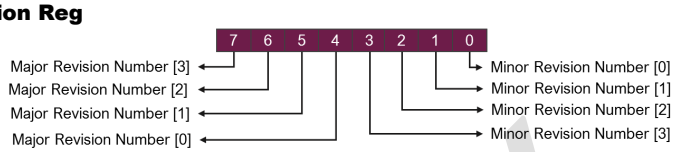
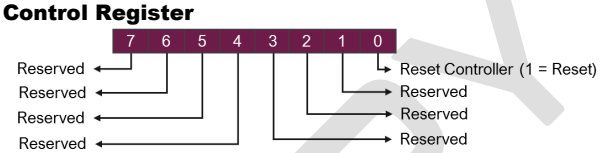
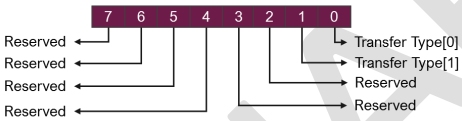
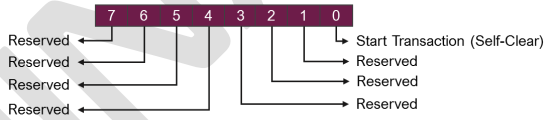
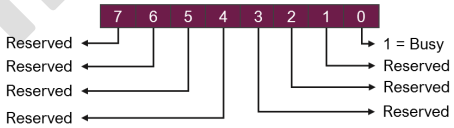
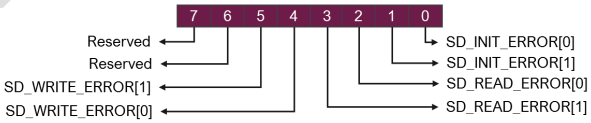
Priority Level & Grouping

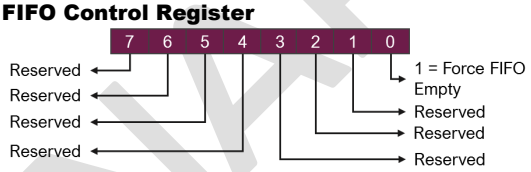
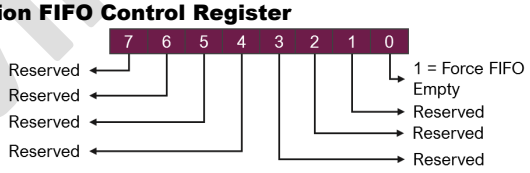
IPL	Priority	Group Definition	VECTORS
111	No Interrupt		
110	Lowest Priority	BEATRIX – DAC	0x58..0x5F – INT Group 2B
101		BEATRIX – IDE/SD, Yamaha	0x50..0x57 – INT Group 2A
100		GAVIN - Timer Group	0x48..0x4F – INT Group 1B
011		GAVIN - SuperIO Group (KB, Mouse, Etc.)	0x40..0x47 – INT Group 1A
010		VICKY Interrupts Auto-Vector (SOF, SOL, Collision, Etc.)	0x1A – INT Group 0A
001	Highest Priority	Not Used in A2560U.	
000	NMI	Not Used	

4. Timer Controllers Registers

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x0200		32	I/O	R/W	**Control Register 0** Value @ Reset: 0x0000_0000 
0x0204		32	I/O	R/W	**Control Register 1** Value @ Reset: 0x0000_0000 
0x0208		32	I/O	R/W	**Timer 0 Value (@ CPU Clock)**
0x020C		32	I/O	R/W	**Timer 0 Compare**
0x0210		32	I/O	R/W	**Timer 1 Value (@ CPU Clock)**
0x0214		32	I/O	R/W	**Timer 1 Compare**
0x0218		32	I/O	R/W	**Timer 2 Value (@ CPU Clock)**
0x021C		32	I/O	R/W	**Timer 2 Compare**
0x0220		32	I/O	R/W	**Timer 3 Value (@ SOF Clock) – Frame Counter**
0x0224		32	I/O	R/W	**Timer 3 Compare**
0x0228		32	I/O	R/W	**Reserved**
0x022C		32	I/O	R/W	**Reserved**

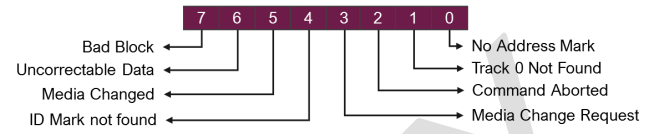
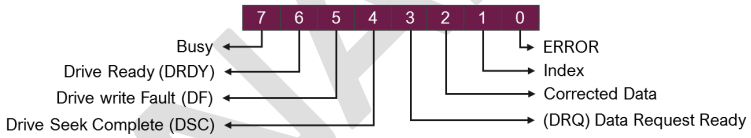
5. SD Card Controller Registers

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x0300		8	I/O	R/W	**Version Reg** 
0x0301		8	I/O	R/W	**Master Control Register** 
0x0302		8	I/O	R/W	**Transfer Type**  Transfer Type [1] [0] Direct Access 0 0 Init SD 0 1 R/W Read SD Block 1 0 R/W Write SD Block 1 1
0x0303		8	I/O	R/W	**Transfer Control Register** 
0x0304		8	I/O	R	**Transfer Status Register** 
0x0305		8	I/O	R/W	**Transfer Error Register**  Init Error [1] [0] / Read Error [1] [0] / Write Error [1] [0] No Error 0 0 / No Error 0 0 / No Error 0 0 Init CMD0 0 1 / Read CMD 0 1 / Write CMD 0 1 Init CMD1 1 0 / Read Token 1 0 / Write Data 1 0 Reserved 1 1 / Reserved 1 1 / Write Busy X X
0x0306		8	I/O	R/W	**Direct Access Data Register** **TX_Data[7:0] (W)** Set TX_DATA prior to starting a DIRECT_ACCESS transaction. Note that the SPI bus has no concept of a read or write transaction. Thus every DIRECT_ACCESS transaction transmits data from the SPI master, and receives data from the SPI slave. **RX_Data[7:0] (R)** Read RX_DATA after completing a DIRECT_ACCESS transaction.
0x0307		8	I/O	R/W	**SD Address Register [7:0]** Normally set to zero, because memory accesses should occur on a 512 bytes boundary. Set the SD/MMC memory address before starting a block read or block write.

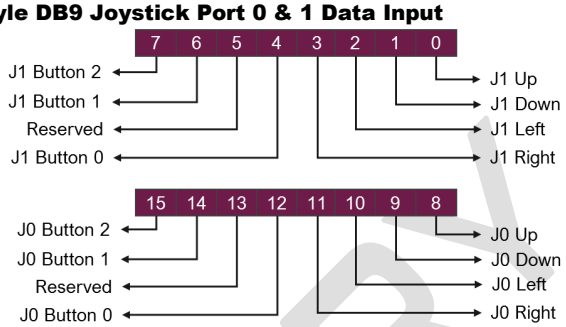
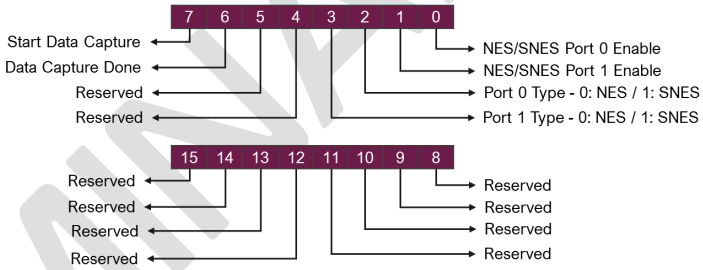
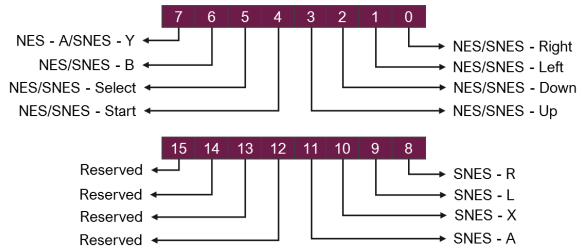
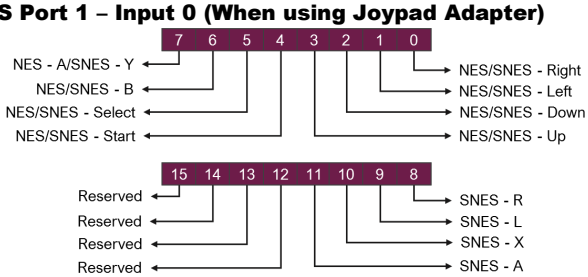
0x0308		**8**	**I/O**	**R/W**	**SD Address Register [15:8]** Normally set SD_ADDR[8] to zero, because memory accesses should occur on a 512 bytes boundary.
0x0309		**8**	**I/O**	**R/W**	**SD Address Register [23:16]**
0x030A		**8**	**I/O**	**R/W**	**SD Address Register [31:24]**
0x030B		**8**	**I/O**	**R/W**	**SPI Clock Del Register** SPI_CLK_DEL controls the frequency of the SPI_CLK after SD initialization is completed. SPI_CLK_DEL = (spiSysClk / (SPI_CLK * 2)) – 1
0x0310		**8**	**I/O**	**R**	**Reception FIFO Data Register** SD/MMC block read data. Note, FIFO size matches the SD/MMC block size of 512 bytes.
0x0312		**8**	**I/O**	**R/W**	**Reception FIFO Data Count Register [15:8]** MSB of FIFO_DATA_COUNT. Indicates the number of data entries within the FIFO.
0x0313		**8**	**I/O**	**R/W**	**Reception FIFO Data Count Register [7:0]** LSB of FIFO_DATA_COUNT. Indicates the number of data entries within the FIFO.
0x0314		**8**	**I/O**	**R/W**	**Reception FIFO Control Register**  Deletes all the data samples within the FIFO. Self clearing.
0x0320		**8**	**I/O**	**R/W**	**Transmission FIFO Data Register** SD/MMC block write data. FIFO size matches the SD/MMC block size of 512 bytes.
0x0324		**8**	**I/O**	**R/W**	**Transmission FIFO Control Register**  Deletes all the data samples within the FIFO. Self clearing.

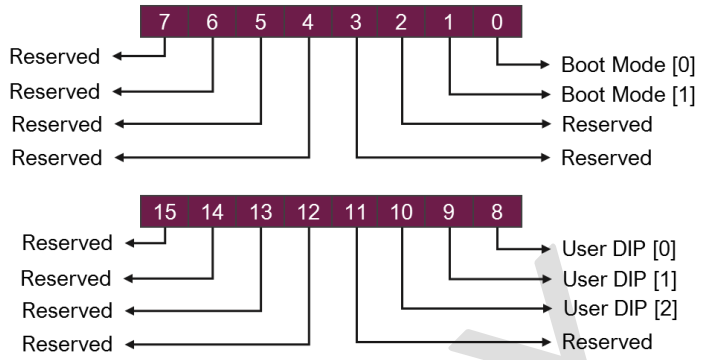
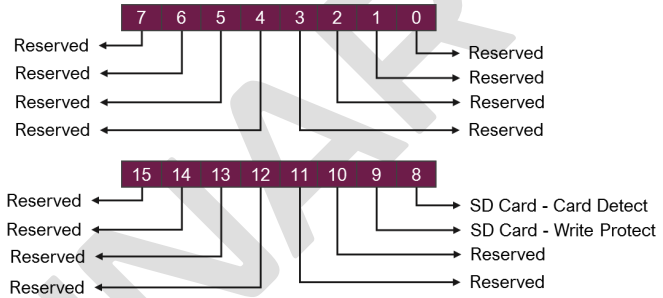
6. IDE Control Registers

(For more detail on how to use the IDE, please consult the official PATA documentation)

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x0400		16	I/O	R/W	IDE Data Register
0x0402		8	I/O	R/W	IDE Error 
0x0404		8	I/O	R/W	IDE Sector CNT
0x0406		8	I/O	R/W	IDE Sector SRT / LBA0
0x0408		8	I/O	R/W	IDE Cylinder Low / LBA1
0x040A		8	I/O	R/W	IDE Cylinder Hi / LBA2
0x040C		8	I/O	R/W	IDE Head / DEVSEL
0x040E		8	I/O	R/W	IDE CMD (W) /STAT (R)  For the Command list, refer to the official PATA Documentation.

7. JOYSTICK Control Registers

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x0500		16	I/O	R/W	**Atari Style DB9 Joystick Port 0 & 1 Data Input** 
0x0502		16	I/O	R	**Reserved -** Reads: 0x0000
0x0504		16	I/O	R/W	**NES/SNES Control Register & Status** 
0x0506		16	I/O	R	**Reserved** - Reads: 0x0000
0x0508		16	I/O	R	**NES/SNES Port 0 – Input 0 (When using Joypad Adapter)** 
0x050A		16	I/O	R	**NES/SNES Port 0 – Input 1 (When using Joypad Adapter)**
0x050C		16	I/O	R	**NES/SNES Port 0 – Input 2 (When using Joypad Adapter)**
0x050E		16	I/O	R	**NES/SNES Port 0 – Input 3 (When using Joypad Adapter)**
0x0510		16	I/O	R	**NES/SNES Port 1 – Input 0 (When using Joypad Adapter)** 
0x0512		16	I/O	R	**NES/SNES Port 1 – Input 1 (When using Joypad Adapter)**
0x0514		16	I/O	R	**NES/SNES Port 1 – Input 2 (When using Joypad Adapter)**
0x0516		16	I/O	R	**NES/SNES Port 1 – Input 3 (When using Joypad Adapter)**

0x0518		**16**	**I/O**	**R**	**DIP Switch Value** 
0x051A		**16**	**I/O**	**R**	**SD Card Write Protect & Card Detect Switch Value** 
0x051C		**16**	**I/O**	**R**	**Reserved -** Reads: 0x5555
0x051E		**16**	**I/O**	**R**	**Reserved -** Reads: 0xAAAA

8. PS2 Controller + Simple UART

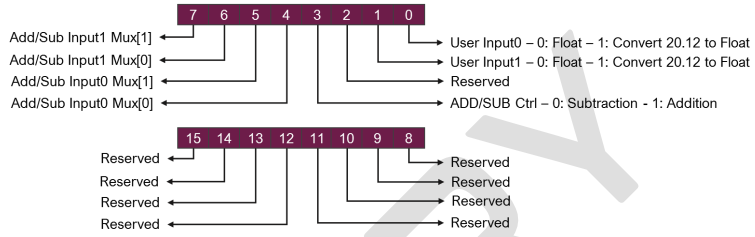
(For more detail on the PS2 Controller, consult the official documentation)
(For more detail on the Simple UART, consult the official 16550 datasheet)

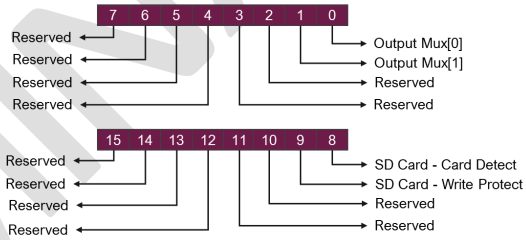
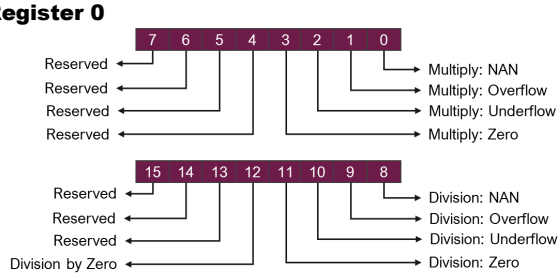
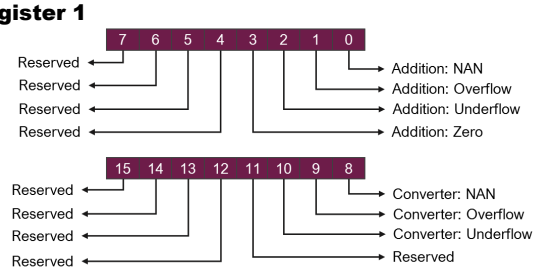
Addy Start Offset	Addy End	Size	Type	R/W	Description
					PS2 Controller
0x2800		8	I/O	R/W	Keyboard/Mouse Output Buffer (W) Keyboard/Mouse Input Buffer (R) Keyboard/Mouse Data Buffer (R/W)
0x2804		8	I/O	R/W	Keyboard/Mouse Status Port (R) Keyboard/Mouse CMD Port (W)
					Simple UART (Compatible with 16550)
0x28F8		8	I/O	R/W	(RHR) Receiver Holding Register (R) (THR) Transmitter Holding Register (W)
0x28F9		8	I/O	R/W	(IER) Interrupt Enable Register
0x28FA		8	I/O	R/W	(ISR) Interrupt Status Register (R) (FCR) FIFO Control Register (FIFO is 16 Bytes Deep) (W)
0x28FB		8	I/O	R/W	(LCR) Line Control Register
0x28FC		8	I/O	R/W	(MCR) Modem Control Register
0x28FD		8	I/O	R	(LSR) Line Status Register
0x28FE		8	I/O	R/W	(MSR) Modem Status Register
0x28FF		8	I/O	R/W	(SPR) Scratch Pad Register
					When DLAB = 1
0x28F8		8	I/O	R/W	(DLL) Baud rate Divisor's Constant LSB
0x28F9		8	I/O	R/W	(DLM) Baud rate Divisor's Constant MSB
0x28FD		8	I/O	W	(PSD) Pre-Scaler Division

9. Fixed-Point Math Processing Block

Addy Start Offset	Addy End	Size	Type	R/W	Description
					UNSIGNED MULTPLICATION
0x3000		32	I/O	R/W	Operand A
0x3004		32	I/O	R/W	Operand B
0x3008		32	I/O	R/W	Results [31:0] Low
0x300C		32	I/O	R/W	Results [63:32] Hi
					SIGNED MULTPLICATION
0x3020		32	I/O	R/W	Operand A
0x3024		32	I/O	R/W	Operand B
0x3028		32	I/O	R/W	Results [31:0] Low
0x302C		32	I/O	R/W	Results [63:32] Hi
					UNSIGNED DIVISION
0x3040		32	I/O	R/W	Operand A
0x3044		32	I/O	R/W	Operand B
0x3048		32	I/O	R/W	Quotient Results [31:0]
0x304C		32	I/O	R/W	Remain Results [31:0]
					SIGNED DIVISION
0x3060		32	I/O	R/W	Operand A
0x3064		32	I/O	R/W	Operand B
0x3068		32	I/O	R/W	Quotient Results [31:0]
0x306C		32	I/O	R/W	Remain Results [31:0]

10. Float-Point Math Processing Block

<table>
<tr><th>Addy Start Offset</th><th>Addy End</th><th>Size</th><th>Type</th><th>R/W</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>Control Registers</td></tr>
<tr><td>0x4000</td><td></td><td>16</td><td>I/O</td><td>R/W</td><td>Control Register 0
 

<table>
<tr><th>Input0 Mux</th><th>[1]</th><th>[0]</th><th>Input 1 Mux</th><th>[1]</th><th>[0]</th><th>Output Mux</th><th>[1]</th><th>[0]</th></tr>
<tr><td>Input Mux 0</td><td>0</td><td>0</td><td>Input Mux 0</td><td>0</td><td>0</td><td>Multiply Out</td><td>0</td><td>0</td></tr>
<tr><td>Input Mux 1</td><td>0</td><td>1</td><td>Input Mux 1</td><td>0</td><td>1</td><td>Division Out</td><td>0</td><td>1</td></tr>
<tr><td>Multiply Out</td><td>1</td><td>0</td><td>Multiply Out</td><td>1</td><td>0</td><td>Add/Sub Out</td><td>1</td><td>0</td></tr>
<tr><td>Division Out</td><td>1</td><td>1</td><td>Division Out</td><td>1</td><td>1</td><td>Value '1' in Float</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>0x4002</td><td></td><td>16</td><td>I/O</td><td>R/W</td><td>Control Register 1
 
</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>Status Registers</td></tr>
<tr><td>0x4004</td><td></td><td>16</td><td>I/O</td><td>R</td><td>Status Register 0
 
</td></tr>
<tr><td>0x4006</td><td></td><td>16</td><td>I/O</td><td>R</td><td>Status Register 1
 
</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>User Input</td></tr>
<tr><td>0x4008</td><td></td><td>32</td><td>I/O</td><td>W</td><td>User Input 0 (IEEE Float Input or 20.12 Fixed-Point Input)</td></tr>
<tr><td>0x400C</td><td></td><td>32</td><td>I/O</td><td>W</td><td>User Input 1 (IEEE Float Input or 20.12 Fixed-Point Input)</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>User Output</td></tr>
<tr><td>0x4008</td><td></td><td>32</td><td>I/O</td><td>R</td><td>User Output (IEEE Float Output)</td></tr>
<tr><td>0x400C</td><td></td><td>32</td><td>I/O</td><td>R</td><td>User Output (Fixed-Point 20.12 Output)</td></tr>
</table>

BEATRIX Address Offset: 0x00B2

11. BEATRIX Control Registers

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x0000			I/O	R/W	TBD
0x0000			I/O	R/W	TBD
0x0000			I/O	R/W	TBD
0x0000			I/O	R/W	TBD
0x0000			I/O	R/W	TBD
0x0000			I/O	R/W	TBD
0x0000			I/O	R/W	TBD
0x0000			I/O	R/W	TBD
0x0000			I/O	R/W	TBD
0x0000			I/O	R/W	TBD
0x0000			I/O	R/W	TBD
0x0000			I/O	R/W	TBD
0x0000			I/O	R/W	TBD

12. PSG (SN76489) Control Registers

(For Detailed information about the part's registers, please consult the SN76489 Datasheet)

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x0110		8	I/O	W	**Internal (FPGA) PSG – LEFT Channel**
0x0120		8	I/O	W	**Internal (FPGA) PSG – RIGHT Channel**
0x0130		8	I/O	W	**Internal (FPGA) PSG – MONO Channel** When writing here, both Channels are written to at the same time.

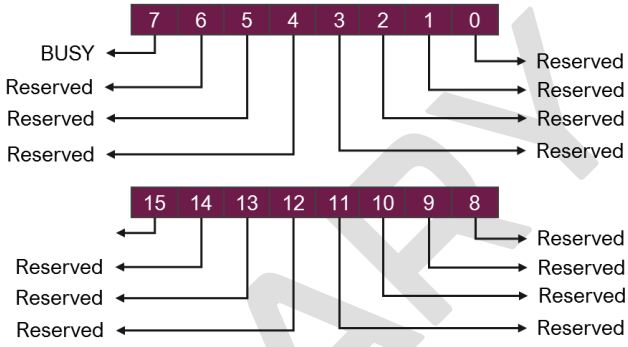
13. OPL3 Control Registers

(For Detailed information about the part's registers, please consult the OPL3 Datasheet)

Addy Start Offset	Addy End	Size	Type	R/W	Description
					RIGHT Channel (Registers summarized)
0x0201		8	I/O	W	**TEST**
0x0202		8	I/O	W	**TIMER-1**
0x0203		8	I/O	W	**TIMER-2**
0x0204		8	I/O	W	**IRQ**
0x0205		8	I/O	W	**Set OPL3 Mode**
0x0208		8	I/O	W	**CSM**
0x0220		8	I/O	W	**AM/VID/EG/KSR/MULT**
0x0240		8	I/O	W	**KSL/TL**
0x0260		8	I/O	W	**AR/DR**
0x0280		8	I/O	W	**SL/RR**
0x02A0		8	I/O	W	**F-Number**
0x02B0		8	I/O	W	**KON/BLOCK/F-Number**
0x02BD		8	I/O	W	**DEPTH/RYTHM**
0x02C0		8	I/O	W	**FEEDBACK**
0x02E0		8	I/O	W	**WAVE/SELECT**
					LEFT Channel (Registers summarized)
0x0301		8	I/O	W	**TEST**
0x0302		8	I/O	W	**TIMER-1**
0x0303		8	I/O	W	**TIMER-2**
0x0304		8	I/O	W	**IRQ**
0x0305		8	I/O	W	
0x0308		8	I/O	W	**CSM**
0x0320		8	I/O	W	**AM/VID/EG/KSR/MULT**
0x0340		8	I/O	W	**KSL/TL**
0x0360		8	I/O	W	**AR/DR**
0x0380		8	I/O	W	**SL/RR**
0x03A0		8	I/O	W	**F-Number**
0x03B0		8	I/O	W	**KON/BLOCK/F-Number**
0x03BD		8	I/O	W	**DEPTH/RYTHM**
0x03C0		8	I/O	W	**FEEDBACK**
0x03E0		8	I/O	W	**WAVE/SELECT**

14. CODEC Control Registers

(For Detailed information about the part's registers, please consult the WM8776SEFT/V Datasheet)

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x0E00		16	I/O	W	**DATA Register** (Data is serialized to the CODEC after the Write Transaction is completed)
0x0E00		16	I/O	R	**STATUS**  Check for the busy flag to go back to '0' before sending another command

15. SID Control Registers

(For Detailed information about the part's registers, please consult the CBM6581 Datasheet)

Addy Start Offset	Addy End	Size	Type	R/W	Description
					LEFT Channel (Registers summarized)
0x1000		8	I/O	R/W	Voice 1 - FREQ LOW
0x1001		8	I/O	R/W	Voice 1 - FREQ HI
0x1002		8	I/O	R/W	Voice 1 – PW LO
0x1003		8	I/O	R/W	Voice 1 – PW HI
0x1004		8	I/O	R/W	Voice 1 - Control
0x1005		8	I/O	R/W	Voice 1 – Attack / Decay
0x1006		8	I/O	R/W	Voice 1 – Sustain / Release
0x1007		8	I/O	R/W	Voice 2 - FREQ LOW
0x1008		8	I/O	R/W	Voice 2 - FREQ HI
0x1009		8	I/O	R/W	Voice 2 – PW LO
0x100A		8	I/O	R/W	Voice 2 – PW HI
0x100B		8	I/O	R/W	Voice 2 - Control
0x100C		8	I/O	R/W	Voice 2 – Attack / Decay
0x100D		8	I/O	R/W	Voice 2 – Sustain / Release
0x100E		8	I/O	R/W	Voice 3 - FREQ LOW
0x100F		8	I/O	R/W	Voice 3 - FREQ HI
0x1010		8	I/O	R/W	Voice 3 – PW LO
0x1011		8	I/O	R/W	Voice 3 – PW HI
0x1012		8	I/O	R/W	Voice 3 - Control
0x1013		8	I/O	R/W	Voice 3 – Attack / Decay
0x1014		8	I/O	R/W	Voice 3 – Sustain / Release
0x1015		8	I/O	R/W	Filter – FC LOW
0x1016		8	I/O	R/W	Filter – FC HI
0x1017		8	I/O	R/W	Filter – RES / FILT
0x1018		8	I/O	R/W	Filter – Mode / VOL
0x1019		8	I/O	R/W	POT X (not Supported)
0x101A		8	I/O	R/W	POT Y (not Supported)
0x101B		8	I/O	R/W	OSC3 / RANDOM
0x101C		8	I/O	R/W	ENV3
0x101D		8	I/O	R/W	Reserved
0x101E		8	I/O	R/W	Reserved
0x101F		8	I/O	R/W	Reserved
					RIGHT Channel (Registers summarized)
0x1200		8	I/O	R/W	Voice 1 - FREQ LOW
0x1201		8	I/O	R/W	Voice 1 - FREQ HI
0x1202		8	I/O	R/W	Voice 1 – PW LO
0x1203		8	I/O	R/W	Voice 1 – PW HI
0x1204		8	I/O	R/W	Voice 1 - Control
0x1205		8	I/O	R/W	Voice 1 – Attack / Decay
0x1206		8	I/O	R/W	Voice 1 – Sustain / Release
0x1207		8	I/O	R/W	Voice 2 - FREQ LOW
0x1208		8	I/O	R/W	Voice 2 - FREQ HI
0x1209		8	I/O	R/W	Voice 2 – PW LO
0x120A		8	I/O	R/W	Voice 2 – PW HI
0x120B		8	I/O	R/W	Voice 2 - Control
0x120C		8	I/O	R/W	Voice 2 – Attack / Decay
0x120D		8	I/O	R/W	Voice 2 – Sustain / Release
0x120E		8	I/O	R/W	Voice 3 - FREQ LOW

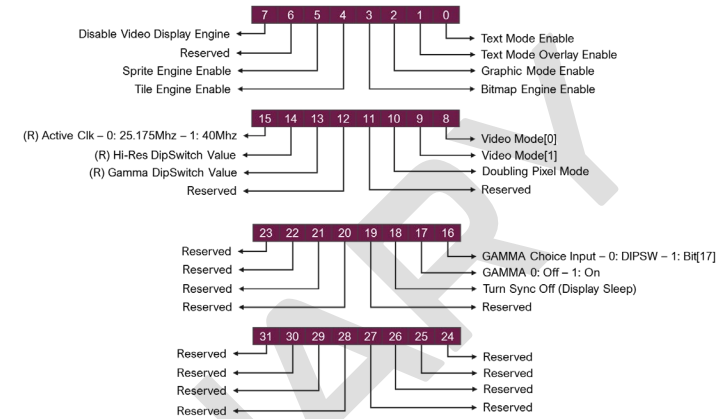
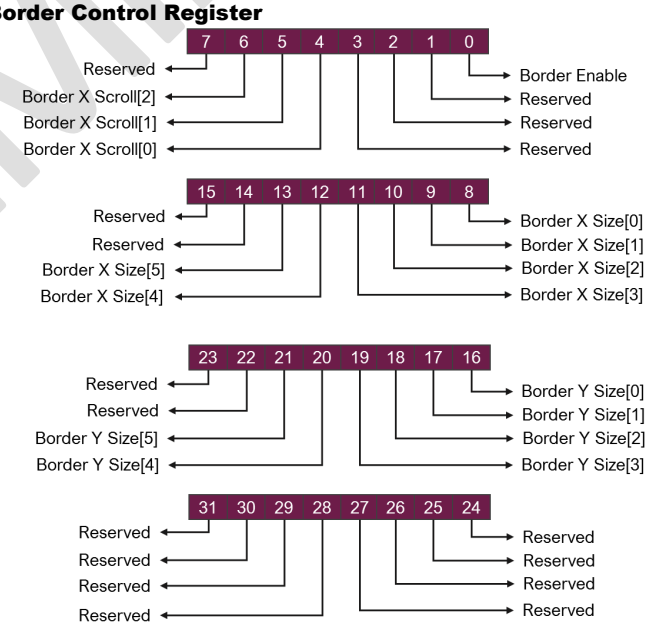
0x120F		8	I/O	R/W	Voice 3 - FREQ HI
0x1210		8	I/O	R/W	Voice 3 – PW LO
0x1211		8	I/O	R/W	Voice 3 – PW HI
0x1212		8	I/O	R/W	Voice 3 - Control
0x1213		8	I/O	R/W	Voice 3 – Attack / Decay
0x1214		8	I/O	R/W	Voice 3 – Sustain / Release
0x1215		8	I/O	R/W	Filter – FC LOW
0x1216		8	I/O	R/W	Filter – FC HI
0x1217		8	I/O	R/W	Filter – RES / FILT
0x1218		8	I/O	R/W	Filter – Mode / VOL
0x1219		8	I/O	R/W	POT X (not Supported)
0x121A		8	I/O	R/W	POT Y (not Supported)
0x121B		8	I/O	R/W	OSC3 / RANDOM
0x121C		8	I/O	R/W	ENV3
0x121D		8	I/O	R/W	Reserved
0x121E		8	I/O	R/W	Reserved
0x121F		8	I/O	R/W	Reserved
					MONO Channel (Registers summarized)
0x1400	0x141F	8	I/O	R/W	When writing here, both Channels are written to at the same time.

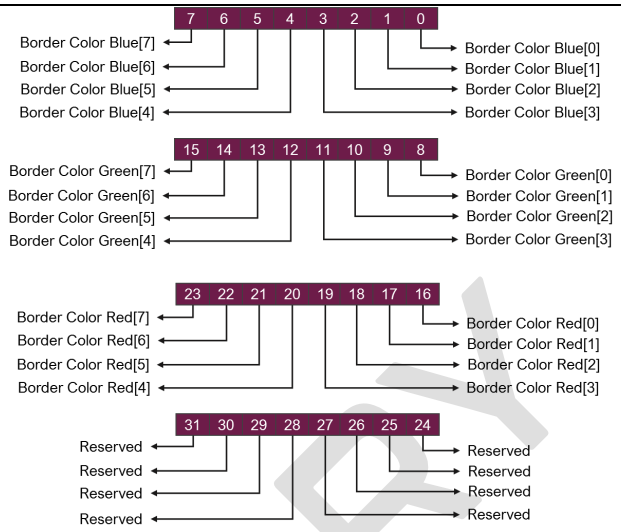
16. DAC Control Registers (48Khz Sampling)

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x2000		8	I/O	R/W	TBD
0x2001		8	I/O	R/W	TBD
0x2002		8	I/O	R/W	TBD
0x2003		8	I/O	R/W	TBD
0x2004		8	I/O	R/W	TBD
0x2005		8	I/O	R/W	TBD
0x2006		8	I/O	R/W	TBD
0x2007		8	I/O	R/W	TBD

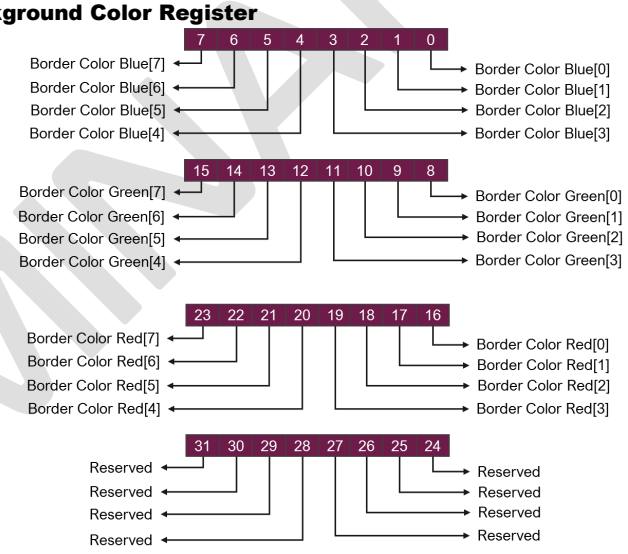
VICKY II Address Offset: 0x00B4

1. System Control Register

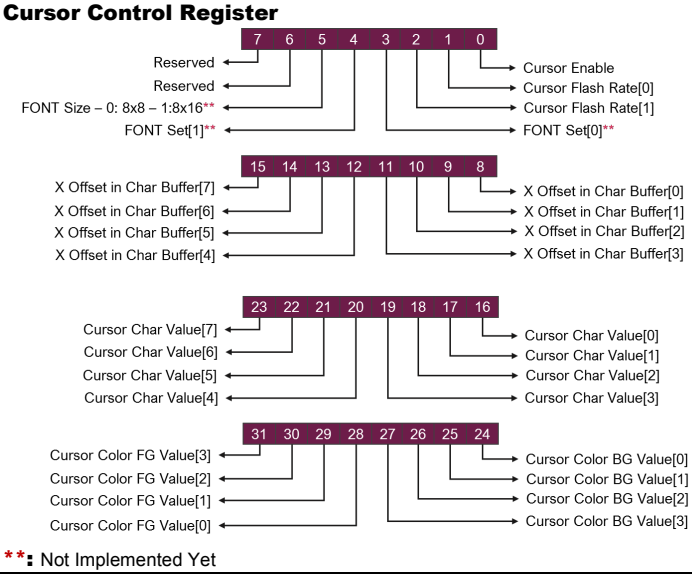
Addy Start Offset	Addy End	Size	Type	R/W	Description
0x0000		32	I/O	R/W	 Video Mode [1] [0] 640x480 @ 60FPS 0 0 800x600 @ 60FPS 0 1 Reserved 1 0 640x400 @ 70FPS 1 1
0x0004		32	I/O	R/W	**Border Control Register** 
0x0008		32	I/O	R/W	**Border Color Register**



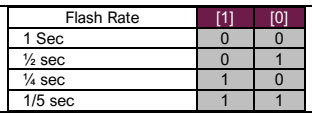
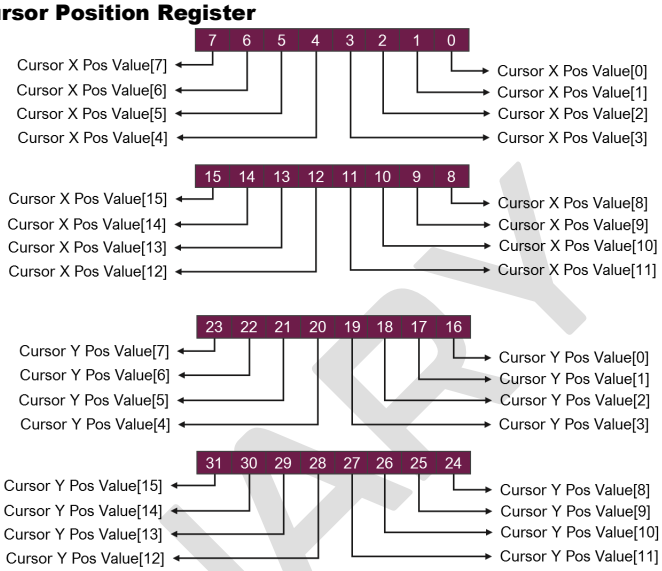
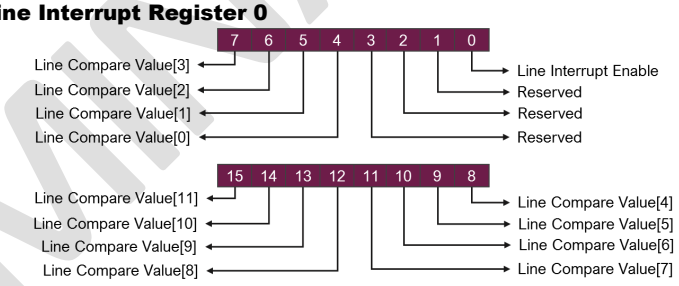
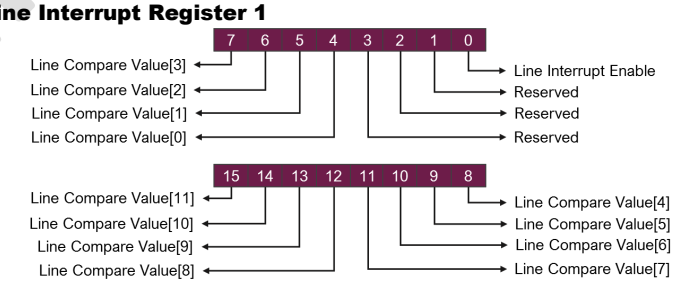
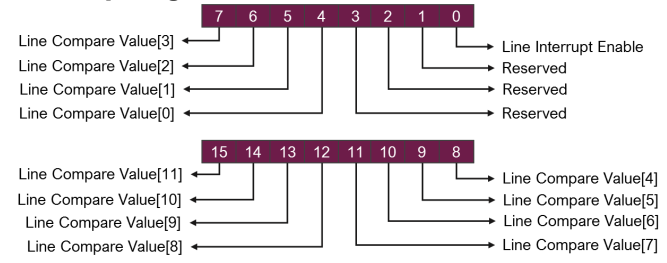
0x000C		**32**	**I/O**	**R/W**	**Background Color Register**

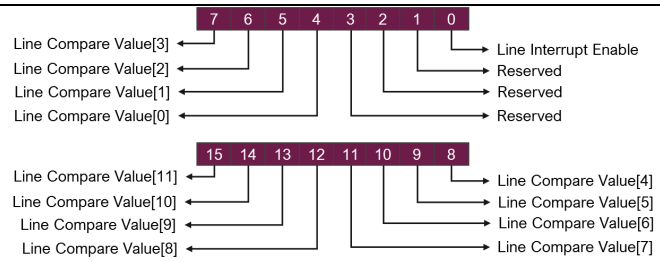


0x0010		**32**	**I/O**	**R/W**	**Cursor Control Register**

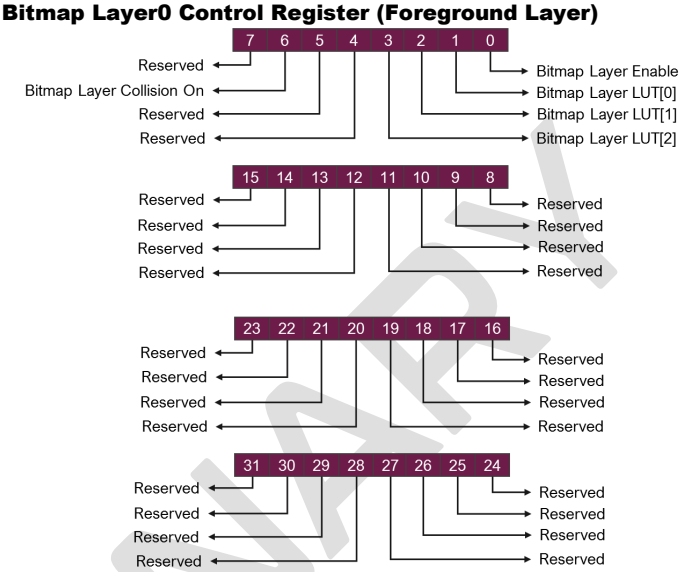
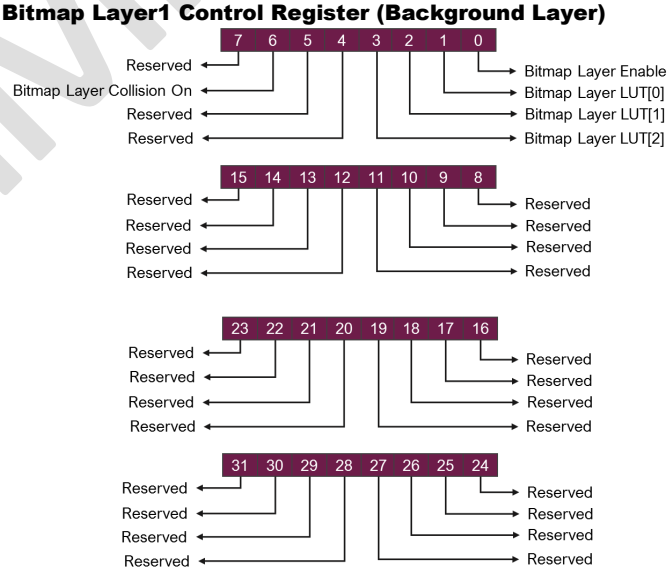


**: Not Implemented Yet

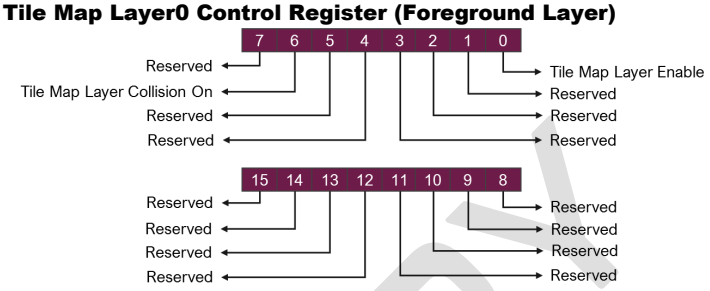
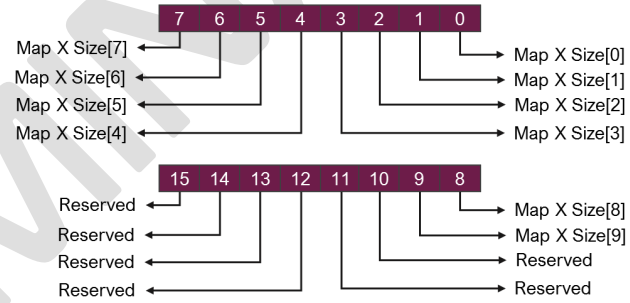
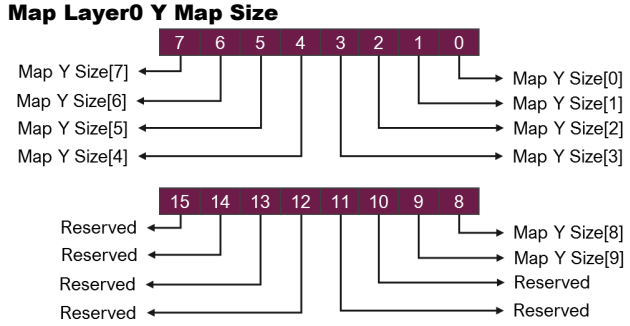
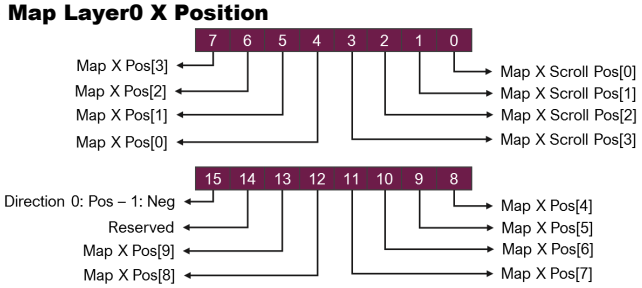
					
0x0014		**32**	**I/O**	**R/W**	**Cursor Position Register** 
0x0018		**16**	**I/O**	**R/W**	**Line Interrupt Register 0** 
0x001A		**16**	**I/O**	**R/W**	**Line Interrupt Register 1** 
0x001C		**16**	**I/O**	**R/W**	**Line Interrupt Register 2** 
0x001E		**16**	**I/O**	**R/W**	**Line Interrupt Register 3**

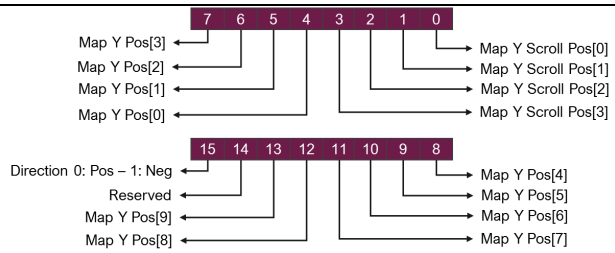
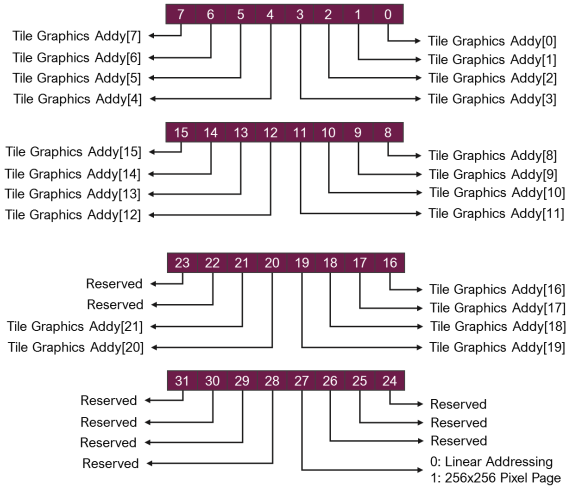
					
0x0020		**16**	**I/O**	**R/W**	**Reserved**
0x0022		**16**	**I/O**	**R/W**	**Reserved**
0x0024		**16**	**I/O**	**R/W**	**Reserved**
0x0026		**16**	**I/O**	**R/W**	**Reserved**
0x0028		**16**	**I/O**	**R/W**	**Reserved**
0x002A		**16**	**I/O**	**R/W**	**Reserved**
0x002C		**16**	**I/O**	**R/W**	**Reserved**
0x002E		**16**	**I/O**	**R/W**	**Reserved**
0x0030		**16**	**I/O**	**R/W**	**FPGA Load Date** 4x BCD Numbers - Year
0x0032		**16**	**I/O**	**R/W**	**FPGA Load Date** 2x BCD Numbers – Month / 2x BCD Numbers Day
0x0034		**16**	**I/O**	**R/W**	**PCB Revision in ASCII** – Example: “A0”
0x0036		**16**	**I/O**	**R/W**	**PCB Revision in ASCII** – Example: “A” + “\n”
0x0038		**16**	**I/O**	**R/W**	**FPGA Sub-Version -** 4x BCD Numbers
0x003A		**16**	**I/O**	**R/W**	**FPGA Version -** 4x BCD Numbers
0x003C		**16**	**I/O**	**R/W**	**FPGA Chip Part Number (low) -** 4x BCD Numbers – “5171”
0x003E		**16**	**I/O**	**R/W**	**FPGA Chip Part Number (hi) -** 4x BCD Numbers – “0009”

1. Bitmap Control Registers

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x0100		32	I/O	R/W	**Bitmap Layer0 Control Register (Foreground Layer)** 
0x0104		32	I/O	R/W	**Bitmap Layer0 VRAM Address Pointer** Offset within the VRAM memory from VICKY's perspective VRAM Address begins @ $00:0000 and ends @ $1FFFFF *Always position the bitmap within a 32bits Boundary address.*
0x0108		32	I/O	R/W	**Bitmap Layer1 Control Register (Background Layer)** 
0x000C		32	I/O	R/W	**Bitmap Layer1 VRAM Address Pointer** Offset within the VRAM memory from VICKY's perspective VRAM Address begins @ $00:0000 and ends @ $1FFFFF *Always position the bitmap within a 32bits Boundary address.*
0x0010		32	I/O	R/W	**Bitmap Collision Layer Control Register** (Not Implemented)
0x0014		32	I/O	R/W	**Bitmap Collision Layer VRAM Address Pointer** (Not Implemented)

2. Tile Map Control Registers

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x0200		16	I/O	W	**Tile Map Layer0 Control Register (Foreground Layer)**  **Note:** The LUT is defined in each tile Attributes Bit field [13:11] The Tile Set is also defined in each tile Attributes bit field [10:8] The Master Collision bit is defined here, but each tile needs to be turn on for collision control by setting bit [14] in the Tile 16bits definition.
0x0204		32	I/O	W	**Tile Map Layer0 VRAM Address Pointer** Offset within the VRAM memory from VICKY's perspective VRAM Address begins @ $000000 and ends @ $1FFFFF *Always position the Map within a 16bits Boundary address.*
0x0208		16	I/O	W	**Tile Map Layer0 X Map Size** 
0x020A		16	I/O	W	**Tile Map Layer0 Y Map Size** 
0x020C		16	I/O	W	**Tile Map Layer0 X Position** 
0x020E		16	I/O	W	**Tile Map Layer0 Y Position**

					
0x0210		**16**	**I/O**	**W**	**Tile Map Layer1 Control Register (Mid-Layer0)**
0x0214		**32**	**I/O**	**W**	**Tile Map Layer1 VRAM Address Pointer** Offset within the VRAM memory from VICKY's perspective VRAM Address begins @ $000000 and ends @ $1FFFFF *Always position the Map within a 16bits Boundary address.*
0x0218		**16**	**I/O**	**W**	**Tile Map Layer1 X Map Size**
0x021A		**16**	**I/O**	**W**	**Tile Map Layer1 Y Map Size**
0x021C		**16**	**I/O**	**W**	**Tile Map Layer1 X Position**
0x021E		**16**	**I/O**	**W**	**Tile Map Layer1 Y Position**
0x0220		**16**	**I/O**	**W**	**Tile Map Layer2 Control Register (Mid-Layer1)**
0x0224		**32**	**I/O**	**W**	**Tile Map Layer2 VRAM Address Pointer** Offset within the VRAM memory from VICKY's perspective VRAM Address begins @ $000000 and ends @ $1FFFFF *Always position the Map within a 16bits Boundary address.*
0x0228		**16**	**I/O**	**W**	**Tile Map Layer2 X Map Size**
0x022A		**16**	**I/O**	**W**	**Tile Map Layer2 Y Map Size**
0x022C		**16**	**I/O**	**W**	**Tile Map Layer2 X Position**
0x022E		**16**	**I/O**	**W**	**Tile Map Layer2 Y Position**
0x0230		**16**	**I/O**	**W**	**Tile Map Layer3 Control Register (Background Layer)**
0x0234		**32**	**I/O**	**W**	**Tile Map Layer3 VRAM Address Pointer** Offset within the VRAM memory from VICKY's perspective VRAM Address begins @ $000000 and ends @ $1FFFFF *Always position the Map within a 16bits Boundary address.*
0x0238		**16**	**I/O**	**W**	**Tile Map Layer3 X Map Size**
0x023A		**16**	**I/O**	**W**	**Tile Map Layer3 Y Map Size**
0x023C		**16**	**I/O**	**W**	**Tile Map Layer3 X Position**
0x023E		**16**	**I/O**	**W**	**Tile Map Layer3 Y Position**
0x0280		**32**	**I/O**	**W**	**Tile Graphics Set Addy Pointer 0** 
0x0284		**32**	**I/O**	**W**	**Tile Graphics Set Addy Pointer 1**

0x0288		32	I/O	W	Tile Graphics Set Addy Pointer 2
0x028C		32	I/O	W	Tile Graphics Set Addy Pointer 3
0x0290		32	I/O	W	Tile Graphics Set Addy Pointer 4
0x0294		32	I/O	W	Tile Graphics Set Addy Pointer 5
0x0298		32	I/O	W	Tile Graphics Set Addy Pointer 6
0x029C		32	I/O	W	Tile Graphics Set Addy Pointer 7

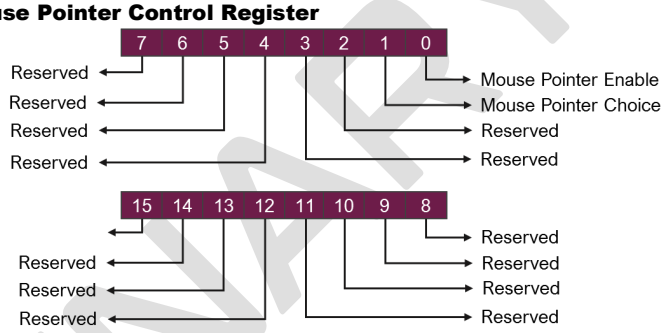
3. Collision Status Registers

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x0300	0x03FF	16	I/O	W	To Be documented

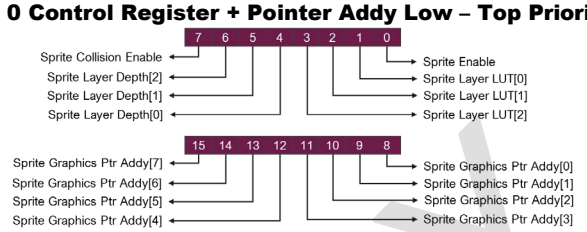
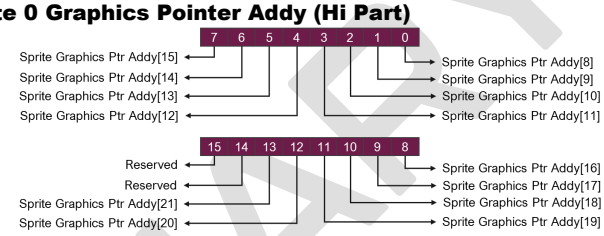
4. Mouse Pointer Graphic Memory

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x0400	0x0BFF	16	MEM	W	16x16 – Full color Mouse Pointer Memory Pointer

5. Mouse Control Registers

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x0C00		16	I/O	R/W	Mouse Pointer Control Register 
0x0C02		16	I/O	R	Mouse Pointer X Position
0x0C04		16	I/O	R	Mouse Pointer Y Position
0x0C06		16	I/O	R	Reserved
0x0C08		16	I/O	R	Reserved
0x0C0A		16	I/O	R/W	PS2 Mouse Byte 0
0x0C0C		16	I/O	R/W	PS2 Mouse Byte 1
0x0C0E		16	I/O	R/W	PS2 Mouse Byte 2

6. Sprites Control Registers

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x1000		16	I/O	W	**Sprite 0 Control Register + Pointer Addy Low – Top Priority** 
0x1002		16	I/O	W	**Sprite 0 Graphics Pointer Addy (Hi Part)**  *Always position the Pointer within a 16bits Boundary address.*
0x1004		16	I/O	W	**Sprite 0 X Position** **Note:** The position 0,0 of a sprite is -32, -32 offscreen
0x1006		16	I/O	W	**Sprite 0 Y Position** **Note:** The position 0,0 of a sprite is -32, -32 offscreen
0x1008	0x100E	16	I/O	W	**Sprite 1**
0x1010	0x1016	16	I/O	W	**Sprite 2**
0x1018	0x101E	16	I/O	W	**Sprite 3**
0x1020	0x1026	16	I/O	W	**Sprite 4**
0x1028	0x102E	16	I/O	W	**Sprite 5**
0x1030	0x1036	16	I/O	W	**Sprite 6**
0x1038	0x103E	16	I/O	W	**Sprite 7**
0x1040	0x1046	16	I/O	W	**Sprite 8**
0x1048	0x104E	16	I/O	W	**Sprite 9**
0x1050	0x1056	16	I/O	W	**Sprite 10**
0x1058	0x105E	16	I/O	W	**Sprite 11**
0x1060	0x1066	16	I/O	W	**Sprite 12**
0x1068	0x106E	16	I/O	W	**Sprite 13**
0x1070	0x1076	16	I/O	W	**Sprite 14**
0x1078	0x107E	16	I/O	W	**Sprite 15**
0x1080	0x1086	16	I/O	W	**Sprite 16**
0x1088	0x108E	16	I/O	W	**Sprite 17**
0x1090	0x1096	16	I/O	W	**Sprite 18**
0x1098	0x109E	16	I/O	W	**Sprite 19**
0x10A0	0x10A6	16	I/O	W	**Sprite 20**
0x10A8	0x10AE	16	I/O	W	**Sprite 21**
0x10B0	0x10B6	16	I/O	W	**Sprite 22**
0x10B8	0x10BE	16	I/O	W	**Sprite 23**
0x10C0	0x10C6	16	I/O	W	**Sprite 24**
0x10C8	0x10CE	16	I/O	W	**Sprite 25**
0x10D0	0x10D6	16	I/O	W	**Sprite 26**
0x10D8	0x10DE	16	I/O	W	**Sprite 27**
0x10E0	0x10E6	16	I/O	W	**Sprite 28**
0x10E8	0x10EE	16	I/O	W	**Sprite 29**
0x10F0	0x10F6	16	I/O	W	**Sprite 30**

0x10F8	0x10FE	16	I/O	W	Sprite 31
0x1100	0x1106	16	I/O	W	Sprite 32
0x1108	0x110E	16	I/O	W	Sprite 33
0x1110	0x1116	16	I/O	W	Sprite 34
0x1118	0x111E	16	I/O	W	Sprite 35
0x1120	0x1126	16	I/O	W	Sprite 36
0x1128	0x112E	16	I/O	W	Sprite 37
0x1130	0x1136	16	I/O	W	Sprite 38
0x1138	0x113E	16	I/O	W	Sprite 39
0x1140	0x1146	16	I/O	W	Sprite 40
0x1148	0x114E	16	I/O	W	Sprite 41
0x1150	0x1156	16	I/O	W	Sprite 42
0x1158	0x115E	16	I/O	W	Sprite 43
0x1160	0x1166	16	I/O	W	Sprite 44
0x1168	0x116E	16	I/O	W	Sprite 45
0x1170	0x1176	16	I/O	W	Sprite 46
0x1178	0x117E	16	I/O	W	Sprite 47
0x1180	0x1186	16	I/O	W	Sprite 48
0x1188	0x118E	16	I/O	W	Sprite 49
0x1190	0x1196	16	I/O	W	Sprite 50
0x1198	0x119E	16	I/O	W	Sprite 51
0x11A0	0x11A6	16	I/O	W	Sprite 52
0x11A8	0x11AE	16	I/O	W	Sprite 53
0x11B0	0x11B6	16	I/O	W	Sprite 54
0x11B8	0x11BE	16	I/O	W	Sprite 55
0x11C0	0x11C6	16	I/O	W	Sprite 56
0x11C8	0x11CE	16	I/O	W	Sprite 57
0x11D0	0x11D6	16	I/O	W	Sprite 58
0x11D8	0x11DE	16	I/O	W	Sprite 59
0x11E0	0x11E6	16	I/O	W	Sprite 60
0x11E8	0x11EE	16	I/O	W	Sprite 61
0x11F0	0x11F6	16	I/O	W	Sprite 62
0x11F8	0x11FE	16	I/O	W	Sprite 63 – Least Priority

7. LUT Memory

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x2000	0x23FF	8	MEM	R/W	LUT0 – 256x 32bits ARGB – Offset 0 is always Transparent
0x2400	0x27FF	8	MEM	R/W	LUT1 – 256x 32bits ARGB
0x2800	0x2BFF	8	MEM	R/W	LUT2 – 256x 32bits ARGB
0x2C00	0x2FFF	8	MEM	R/W	LUT3 – 256x 32bits ARGB
0x3000	0x33FF	8	MEM	R/W	LUT4 – 256x 32bits ARGB
0x3400	0x37FF	8	MEM	R/W	LUT5 – 256x 32bits ARGB
0x3800	0x3BFF	8	MEM	R/W	LUT6 – 256x 32bits ARGB
0x3C00	0x3FFF	8	MEM	R/W	LUT7 – 256x 32bits ARGB

8. GAMMA LUT Memory Blocks

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x4000	0x40FF	8	MEM	R/W	GAMMA Correction Blue Channel
0x4100	0x41FF	8	MEM	R/W	GAMMA Correction Green Channel
0x4200	0x42FF	8	MEM	R/W	GAMMA Correction Red Channel

9. FONT Memory Block

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x8000	0x8FFF	8	MEM	R/W	FONT Character Graphics Storage

VICKY II Address Offset: 0x00B6

10. Text Memory Block

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x0000	0x3FFF	8/16	MEM	R/W	Text Mode Character Display Memory

11. Text Color Memory Block

Addy Start Offset	Addy End	Size	Type	R/W	Description
0x8000	0xBFFF	8/16	MEM	R/W	Text Mode Color Display Memory

12. Text Color LUT

Addy Start Offset	Addy End	Size	Type	R/W	Description
0xC400	0xC43F	8/16	MEM	R/W	16x 32Bits Values ARGB for Foreground Colors
0xC440	0xC47F	8/16	MEM	R/W	16x 32Bits Values ARGB for Background Colors